What is claimed :

1. A memory device comprising:
an array of memory cells coupled to even and odd local bit lines; and
select transistors to couple the even local bit lines to even global bit lines and to couple the odd local bit lines to odd global bit lines.

2. The memory device of claim 1 wherein the local bit lines are positioned approximately parallel with each other and are sequentially numbered.

3. The memory device of claim 1 wherein the global bit lines are positioned approximately parallel with each other and are sequentially numbered.

4. The memory device of claim 1 and further comprising:
a first multiplexer circuit including some of the select transistors; and
a second multiplexer circuit including the remaining select transistors, wherein the array of memory is positioned between the first and second multiplexer circuits.

5. The memory device of claim 4 wherein the first and second multiplexer circuits comprise four select transistors coupled between an associated local bit line and an associated global bit line, each select transistor having a control gate.

6. The memory device of claim 5 and further comprising:
a first select line coupled to control gates of the select transistors that are coupled to a first and a second local bit line of the even local bit lines; and
a second select line coupled to control gates of the select transistors that are coupled to a first and a second local bit line of the odd local bit lines.

7. The memory device of claim 1 wherein each of the memory cells is a flash memory cell that is comprised of a floating gate capable of holding a charge.

8. The flash memory system of claim 7 wherein a presence or absence of the charge determines a state of the flash memory cell.

9. A memory device comprising:

an array of memory cells coupled to a plurality of bit lines divided into even and odd local bit lines;

a plurality of global bit lines that are divided into even and odd global bit lines;

a multiplex circuit comprising four select transistors coupled between an associated local bit line and an associated global bit line, each select transistor having a control gate, the multiplex circuit selectively coupling the even local bit lines to the even global bit lines and the odd local bit lines to the odd global bit lines;

a first select line coupled to control gates of the select transistors that are coupled to the even local bit lines; and

a second select line coupled to control gates of the select transistors that are coupled to the odd local bit lines.

10. The memory device of claim 9 wherein there are twice as many of the plurality of local bit lines as the plurality of global bit lines.

11. The memory device of claim 9 wherein the plurality of local bit lines are formed on a first metal level and the plurality of global bit lines are formed on a second metal level.

12. The memory device of claim 9 wherein the system is manufactured such that the plurality of local bit lines are on a different level than the plurality of global bit lines.

13. The memory device of claim 9 wherein the array of memory cells is floating gate memory cells arranged in rows and columns.

14. A method of operating an integrated circuit memory comprising:
selectively coupling odd local bit lines to odd global bit lines; and
selectively coupling even local bit lines to even global bit lines.

15. The method of claim 14 wherein select transistors are coupled between the local bit lines and the global bit lines.

16. The method of claim 14 wherein selectively coupling odd local bit lines comprises coupling a first group of alternating local bit lines to a first global bit line and selectively coupling even local bit lines comprises coupling a second group of alternating local bit lines to a second global bit line.

17. The method of claim 14 wherein selectively coupling odd local bit lines comprises activating a first select transistor that is coupled between a first even local bit line and a first even global bit line.

18. The method of claim 14 wherein selectively coupling comprises:
generating an activation signal coupled to a control gate of a select transistor; and
the select transistor coupling a first even local bit line to a first even global bit line in response to the activation signal.

19. The method of claim 14 wherein selectively coupling comprises:
generating a plurality of activation signals, each signal coupled to a different select transistor of a plurality of select transistors; and
the plurality of select transistors selectively coupling the even local bit lines to the even global bit lines and the odd local bit lines to the odd global bit lines in response to the activation signals.

20. The method of claim 14 wherein the integrated circuit memory is a flash memory device.